17. A method of fabricating an integrated circuit, comprising the steps of:

forming a pre-metal dielectric (PMD) layer over a semiconductor body;

forming a contact hole in said PMD layer;

depositing a liner layer over said PMD layer including in said contact hole using physical vapor deposition, wherein said liner layer has an overhang portion at a top of said contact hole;

performing a sputter etch using a low bias to at least reduce a thickness of said overhang portion;

depositing a barrier layer over said liner layer; and

depositing a metal filler to fill said contact hole.

18. The method of claim 17, wherein said step of depositing a barrier layer comprises PVD and occurs prior to said step of performing a sputter etch.

19. The method of claim 17, wherein said metal filler comprises tungsten.

20. The method of claim 17, wherein said metal filler comprises CVD TiN.

21. The method of claim 17, wherein said liner layer comprises Ti and barrier layer comprises TiN.

22. The method of claim 17, wherein said low bias is in the range of 0 to –300 volts.